J. Thomas Pawlowski
Fellow and Chief Technologist
Micron Technology, Inc.

J. Thomas Pawlowski is a Fellow and Chief Technologist with Micron's Architecture Development Group. His responsibilities include evaluating new technologies and investments, exploring new memory and system architectures, and providing guidance to many technical teams, both internally and external to Micron.

Mr. Pawlowski's experience includes the creation or co-creation of numerous groundbreaking memory architectures and concepts including: synchronous burst pipelined SRAM; hierarchical cache systems; Zero Bus Turnaround SRAM; abstracted memory; the first double data rate memory (starting with SRAM and extending to DRAM and NAND technologies); Pseudo-Static RAM; high-speed NAND; the first double address rate memory; the first quad data rate memory; the first multi-channel memory; memories on SERDES buses; RLDRAM (the first DRAM to exceed SRAM performance); refresh and error correction schemes for memory subsystems; the first 3D memory concept; root hardware architecture of Micron's newly nondeterministic Finite Automata Processor; abstraction protocols, new ECC concepts, 3D Xpoint system architectures and other projects to be announced.

Mr. Pawlowski earned a bachelor of applied science degree in electrical engineering, *summa cum laude,* from the University of Waterloo in Canada. He has well over 100 U.S. and in-flight patents and serves on several advisory boards and conference program committees.

In his spare time, Mr. Pawlowski designs and builds loudspeakers, simulation tools, fabrication tools, and he has completed 68% of the design and fabrication of a high-efficiency electric concept car.